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EFFLUENT MONITORING FOR NUCLEAR SAFEGUARDS†

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ABSTRACT

A microprocessor-based instrument operates a continuous surveillance on effluents from a nuclear facility. It receives and evaluates pulses from two NaI detectors and a set of single-channel analyzers. It has self-diagnosing capability so that it takes actions not only when it recognizes excessive radioactivity but also when it ascertains some abnormal behaviour. Power failure procedure and automatic restart are provided. Operative constants such as alarm thresholds, times, and number of successive measurements are permanently stored in a read/write battery operated C-MOS memory. The program allows automatic succession of phases in a peculiar way and has a feature for loading an auxiliary program into RAMs.

1. Introduction

An automatic instrument for monitoring effluents from a plutonium facility is described. Monitoring is performed both for safety sake and for nuclear safeguards in order to avoid possible diversions from this way.

The instrument contains an Intel* Single Board Computer type SBC 80/10 and operates autonomously without the need of any surveillance. It has self-diagnosing capability so that it can ascertain if both the effluent radioactivity is kept within the norm and its own operation is behaving correctly. An endless succession of measurement cycles interrupted by calibration procedures is performed. Times for each one of the measurements in a series as well as the interval between calibrations are selected by the operator during initialization.

The normal operation relies on the comparison of the measured values with prefixed limits, without taking any initiative if limits are not exceeded. In case of higher radioactivity or wrong behaviour, some actions are automatically initiated and alarms are set up.

The operator is called only during alarm conditions, but during normal periods the instrument is operated 24 hours a day and no intervention is needed. Suitable warning to the building computer is given both in case of alarm or in case of local power failure.

2. Generality

The instrument consists of two analog chains connected to two NaI detectors with photomultiplier tubes and a digital part controlled by a microprocessor Intel 8080A. Each one of the analog chains contains a preamplifier, an amplifier, a stabilizer, and some single-channel analyzers (SCAs). The chain is simply assembled with commercial NIM modules and needs not to be described in detail. The NaI detectors have different sizes to perform different tasks. One, used for low energy gamma particles (FIDLER), has a diameter of 127 mm (5") and a thickness of 1.50 mm (1/16"), while the second one, used for medium energy particles, has diameter and thickness of 50.8 mm (2" x 2").

Both detectors are immersed in the liquid (Fig. 1) of a suitable vessel kept completely filled by the geometry. The impurity content in the liquid is kept uniform by a continuously operated stirring mechanism.

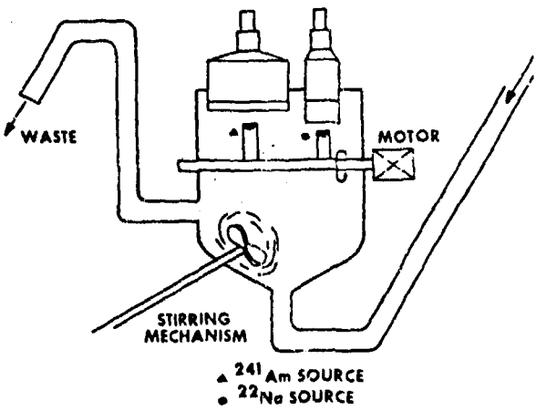

Fig. 1. Assembly of detectors and sources in the vessel.

In Fig. 2 the spectrum of a 94.2% ^{239}Pu sample is reported[1] as it is obtained with both a Ge(Li) and a NaI detector. The problem of using the most suitable detector or detectors has been debated. Germanium detectors, both of the lithium-drifted and the intrinsic type have been taken into consideration. The principal objective was to detect and measure accurately the 17 keV gamma particles consequent to alpha emission. Other energies of interest[2] are the 50.6 keV peak and the region of 400 keV, which is resolved in many peaks with Ge and develops a broad bump with NaI. The self-absorption of the liquid (water) has been taken into account, examining the most appropriate type and geometry of the detector. We should remember that 1 cm of

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‡ On leave from Euratom Joint Research Center, Ispra, Italy.
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water is stopping about 80% of the 17 keV radiation.[3] To obtain the highest effectiveness the detectors must be immersed in the liquid and protected by a very thin berillium window. Unfortunately the liquid will corrode the Be window in the long run if a suitable protection is not provided. For that purpose a special rubber cap is added, and this reduces the 17 keV rate of about 10%.

The final decision has been taken upon the basis of the experience of the Nuclear Safeguard group of the Laboratory. The thin NaI detector has proved to be very well suited to stop the low energy particles without being severely disturbed by Compton background of higher energy particles. In addition NaI detectors can be easily obtained with fairly large active areas so that an adequate pulse rate in the 17 keV range can be achieved. On the contrary it is quite hard to achieve the same active surface with Ge detectors. Apart from problems of cooling and protecting, even in case of coaxial detectors completely immersed in the liquid, the effect of viewing solid angle limits the efficiency since the detectors are physically separated

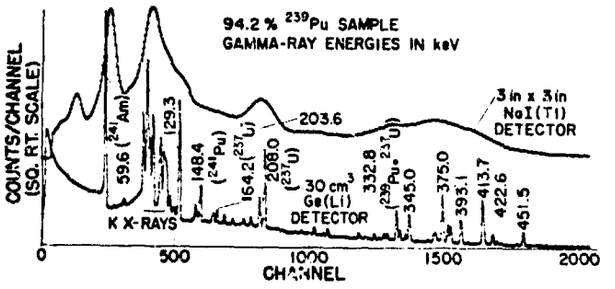

Fig. 2. Comparison of plutonium gamma-ray spectra from 30 cm^3 Ge(Li) detector and 76 x 76 mm NaI detector. Note the square root scale (from Ref. 1).

from the liquid by the surrounding vacuum. For these reasons NaI detectors were selected. As a consequence only the integral counting in the region of interest instead of a full spectrum will be acquired.

The peak areas are corrected for background[1,4] with the simple "two window" method instead of the three windows method that is usually taken in evaluating peaks from a Ge detector spectrum. A single-channel analyzer (SCA) is centered on the peak of interest and a second SCA is set in a nearly flat zone for background measurement. The total area A is evaluated by that with the equation:

$$A = P - (n/n_1) \cdot kB \qquad (1)$$

where P is the total measured activity under the peak, and B is the activity in the background region; n and n_1 are number of channels in the two measurements, and k is a correction factor depending on the slope of the background and is determined during the system calibration.

Using equal channel width for peak and background the simple relation is obtained:

$$A = P - kB \qquad (2)$$

and this is the evaluation that the microprocessor is instructed to perform.

Each one of the two chains carries out an associated measurement of background and contains a suitable gamma source for proper calibration. The thin detector is used to measure only the 17 keV peak and associated background and uses an ^{241}Am source for calibration (calibrating energy 59.6 keV). The thick detector is used to measure the 59.6- and 400-keV peaks plus background and uses a ^{22}Na source (calibrating energy 511 keV).

Three different types of alarms have been taken into consideration and will be better described in the following:

ALARM 1 if the radioactivity in the 17 keV peak exceeds the maximum tolerable intensity

ALARM 2 if something is going wrong with the calibration procedure

ALARM 3 in case of lack of power.

3. Choice of the System

Depending on the use of NaI or Ge detectors and on the use of CAMAC standard or special design, four different systems have been examined. They are reported in Figs. 3 through 6. The first option (Fig. 3) is the chosen system and will be described thoroughly.

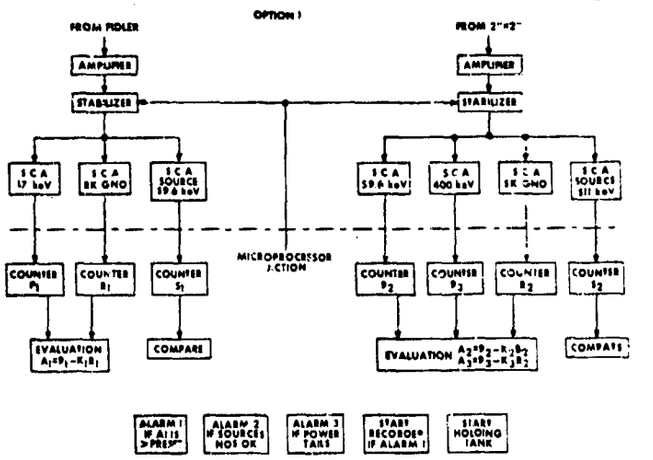

Fig. 3. Block diagram of the adopted option using two NaI detectors and an ad hoc assembly

Figure 4 shows a Ge option based on the use of a single analog chain, a digital stabilizer, and an ADC for a full spectrum acquisition. The calibration set up utilizes the 413.7 keV peak contained in ^{239}Pu spectrum. In Fig. 5 the Ge option is based on CAMAC. Some commercial CAMAC modules can be purchased solving part of the problems. Finally, Fig. 6 shows the NaI CAMAC option where the seven SCAs are connected to a single CAMAC 8-fold scaler. In this block diagram the chosen crate controller is a commercial one, microprocessor based, that matches the requirements needed for autonomous operation with the possibility of being included in a CAMAC parallel branch or in a CAMAC serial loop.

This stand-alone instrument seems not particularly suitable for CAMAC; nevertheless its employment in an integrated system controlled by a central computer should render CAMAC quite attractive. The power of

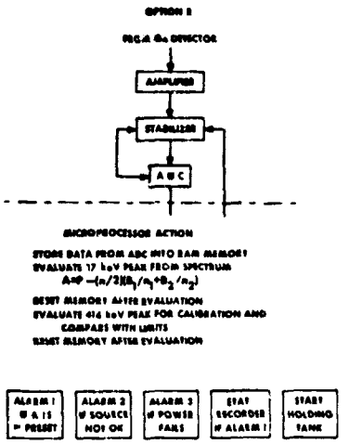

Fig. 4. Block diagram using a Ge detector and analog-to-digital converter.

CAMAC in designing, updating and reusing parts of the system is well expressed in Ref. 5, from where I wish to take some words to agree that CAMAC has saved a lot of money "in eliminating duplicate engineering efforts in the laboratories, in simplifying implementation of modules and systems in the field and in lowered maintenance costs." This probably would have been the case if all the surrounding instrumentation had been designed to profit from the benefits of an integrated system. But different projects were already running so the logic consequence was to abandon the idea of using CAMAC. As this self-operated equipment is not very meaningful in CAMAC if not framed in a bigger system, I preferred to make a design directly optimized for the task.

4. Hardware Design

The instrument is made according to the block diagram of Fig. 3. It is contained in two rack-mounted crates: 1) a standard NIM bin for the analog chains, and 2) a three-unit chassis containing a single-board computer Intel SBC 80/10, the suitable hardware for operation, counting, and evaluation, and the power supply.

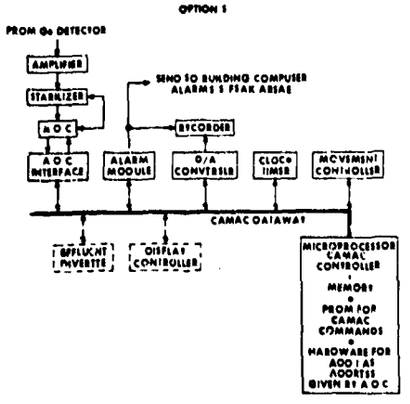

Fig. 5. CAMAC application of the setup of Fig. 4

The choice of the single-board computer SBC 80/10, based on the popular 8080A microproceasor, is due to the fact that it contains all the necessary features for the syster, i.e., PROM and RAM memory, parallel and serial interfaces. The PROM size is very suitably matched because 4k bytes (4096) are provided and the actual program occupies about 4000 bytes. The 1k-byte RAM of the board is more than sufficient for the instrument because only SCAs are used without full spectrum acquisition. The two parallel interfacea assembled on the board are used respectively, one for interrupts and input data and the other for output data. The USART allows for serial input/output communications with an interactive terminal. A suitably quartz-driven clock is self-contained on the board and is also used in the other circuitry via a C-MOS dividing chain. The only limitation of the SBC 80/10 is that only one of the 8 levels of interrupt conceived for the Central Processor Unit (CPU) is decoded. That compels the unit to follow up to recognize the interrupt sources.

All the hardware external to the SBC 80/10 is designed with SSI and MSI and only a few parts will be illustrated. Generally 74LS series and C-MOS chips

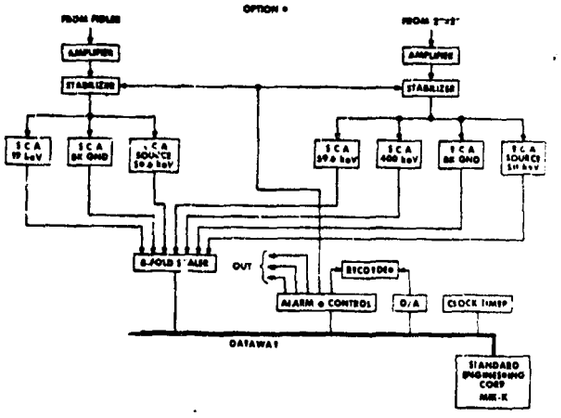

Fig. 6. CAMAC assembly with NaI detectors and crate controller that can be linked in wider frames.

are used. They are assembled in a high density wire-wrapped board that has been programmed for a punched tape-driven wire-wrap machine. The salient parts of the hardware perform the following operations:

- Action in case of power failure and automatic power restart
- C-MOS storing of constants for permanent memorization
- Memory-mapped logic
- Enable and disable of the circuitry
- Processing of pulses
- Operative fields (software controlled)
- Timing and interrupts
- Alarms
- Source displacement for calibration

— Digital to analog conversion and start chart recorder

— Front panel and remote indications

— Optical isolation between the instrument and the external features

Some of the details will be explained in the following.

5. Power Failure and Automatic Power Restart

Particular care has been dedicated to power failure and automatic restart. A suitable threshold on the dc supply voltage will set up the alarm to the building computer and stop the instrument before the voltage goes below safety values. The restart is operated with a suitable hysteresis that allows the voltage to regain nearly the final value. A suitable switch allows the operator to decide if the automatic restart is used. The program will read the position of the switch and take the appropriate action.

Two different conceptions have been examined depending on how interrupts, reset, and stop command are operated. The first one had power failure and automatic restart setting a program interrupt, while the stop feature was simply disabling the circuitry and resetting the CPU. The second one on the contrary relies on a dc reset of the CPU and all the circuitry if the voltage is lower than the prefixed value. Obviously the program counter restarts automatically from zero when the power returns. The stop command becomes inefficient if used for resetting so that an interrupt procedure is necessary to serve the stop command.

Both solutions have been carried out completely and tested. The first one had Schmitt triggers and time constants so that a careful setup was necessary. Times were proportioned in such a manner that it was impossible to start a power failure procedure without a successive restart even in case of successive short breaks in the power line. The second solution exploits the fact that a battery-operated +5.4V dc supply is permanently present for the C-MOS RAM. It is based on the use of a comparator without any time constant so that its intervention is almost immediate, thus avoiding phase problems in case of successive breaks.

Figure 7 shows the circuit with the comparator, where the +5.4V voltage is brought to one input via a divider, and the normal +5V supply goes to the other input with a suitable feedback that allows for a hysteresis of about 5% of the voltage. The comparator output drives a flip-flop that is dc connected directly or indirectly to all the circuitry and the CPU. So when power is going up, a dc reset is initializing all the bistable circuits and keeps the CPU reset up to when the comparator output voltage swings. At this point the program counter is released from zero and begins the initialization of the interface circuits and starts the clock of the instrument if APRE = 1, i.e., if the automatic power restart switch is enabled. The program comes then to a halt, waiting for interrupts that will arrive automatically from the clock or from the pulses processed by the analog chains. The various phases consequent to clocks are described in paragraph 7.

The automatic power restart will restore the operation with all the operative variables. That caused some difficulty during the design stage because no core memory is present in the system. The purpose is to give the operator the possibility to set some constants such as times, thresholds, number of measurements between calibrations, to values that can be changed along the necessities. If these values are written as part of the program into the PROMs, they will become invariant. If these values are stored into RAMs, they will disappear with the power so that they cannot be retraced when the power comes back. The problem has been solved using a C-MOS RAM to store the variables and a small Ni-Cd battery directly powered by the +12v supply of the instrument via a high value resistor, a parallel Zener diode and a series diode. The current drain of the C-MOS RAM from the +5.4V battery during stand-by periods is so small that it can be out of operation for months without losing the stored information.

6. Pulse Counting and Memory-Mapped Logic

The expected pulse rate of pulses coming from the analog chains is so low that counters at the output of the SCAs are unnecessary. The hardware allows each pulse coming from the 5 SCAs (three peaks and two backgrounds) to establish an interrupt request that is served after suitable polling. Software controlled gates are enabled only during the appropriate phase. Reset of each counter is performed by program at the beginning of each measurement. Preferential hardware routing is given to 17 keV pulses in order to avoid a loss of any one of these pulses in case of simultaneousness.

The higher rate corresponding to source pulses does not allow the storing of each pulse into the RAM memory through a program interrupt. Pulses coming from the 2 SCAs centered on the peaks corresponding to

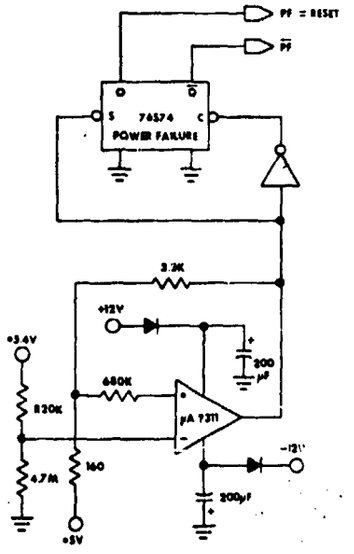

Fig. 7. Power failure detector. The 5.4V supply is battery operated and will never disappear. The negative going output from comparator occurs at a voltage of about 4.65V and sets power failure flip-flop that disables all the circuitry. When power returns, PF flip-flop will keep the circuits at reset until the voltage reaches about 4.9V.

the source emissions are counted in two 16-bit counters. The two counters are seen as part of the memory and are connected to the data bus via tristate buffers. A flip-flop will be set if during counting one or both counters will overflow. The program will recognize the overflow as a reason for alarm.

During source counting the analog chain stabilizers are activated. They will compensate for drifts occurring anywhere from the NaI detector-PM tube assembly to the amplifier output. They will keep constant the amplitude of the pulses corresponding to the source peak.

The memory-mapped logic will include in the memory addresses not only the counters but also some bistable circuits called operative fields as explained below. Table I reports all the addresses in hexadecimal (and decimal) form used within the instrument, including the addresses for PROMs and RAMs contained in the single-board computer and already prefixed by the manufacturer. Hardware uses incomplete decoding.

Operative fields (OP fields) are read/write bytes that are used by the program to control the hardware. The phases of the operation are contained in OP1. The least significant bit (read only) is connected to the APRE switch and is used by the program to decide if the automatic restart has to be done. Write and read in OP1 can be different. For example, the START command gives the hexadecimal value 44, but it is read as 04 and used for starting the calibration procedure; CONTINUE will write the value 60H and will be read as 20 to start the MEASurement phase. The attempt to start source counting (write 08H) or start pulse counting (write 20H) can result in alarm if the source movements were not properly confirmed (see Fig. 11). They can be read as Alarm 21 or Alarm 23, respectively. Operative field OP2 contains other commands and service flags. TEST and PRINT flags are used respectively to create odd conditions without sending alarms

TABLE I

ITEM	HEX ADDR.	DECIMAL ADDR.
On Board PROMs	0000 - 0FFF	0 - 4095
On Board RAMs	3C00 - 3FFF	15360 - 16383
C - MOS RAM	4000 - 40FF	16384 - 16639
Counters & OP Fields	8000 - 8007	32768 - 32775

to the building computer and to print data from source counters and from pulse counters. They are always reset by hardware at the beginning of each measurement to avoid the possibility of forgetfulness that will result in the very dangerous lack of warning to the building computer or in a mass of unuseful printing of data.

The total memory-mapped logic in the range of 8000H addresses is reported in Table II. Operative fields OP3 and OP4 are only used for writing Alarm 1 or Alarm 22, if any, corresponding to pulse or source counting.

7. Timing and Flow Charts

The timing is controlled by an instrument clock occurring every 30 s as explained. This is obtained by a C-MOS dividing chain from the 2.048 MHz quartz-controlled clock of the SBC 80/10. All the dividers are dc reset if enable flip-flop is not set due to program requirements or to power failure. When a start is given by the operator, the reset is released and the first clock will occur after 30 s, determining the succession of phases. The first phase is normally

TABLE II

BIT ASSIGNMENT

ADDRESS (HEX)	BIT NO.	WRITE	HEX VALUE	BIT NO.	READ
8000	0-7	READ ONLY COUNTERS			SC 1 (Low)
8001	8-15				SC 1 (High)
8002	0-7				SC 2 (Low)
8003	8-15				SC 2 (High)
8004	0	-	01H	0	APRE
(OP1)	1	Warm up	02H	1	Warm up flag
	2	MOV1	04H	2	MOV1 flag
	3	Source Count Enable (Alarm21?)	08H	3	SC flag
	4	MOV2	10H	4	MOV2 flag
	5	MEAS (Alarm23?)	20H	5	MEAS flag
	6	SET E	40H	6	AL21
	7	-	80H	7	AL23
START	(2,6)	SET E + MOV1	44H	(2)	Read 04H
CONTINUE	(5,6)	SET E + MEAS	60H	(5)	Read 20H
8005	0	TEST	01H	0	TEST
	1	COUNT ENABLE (1/0)	02H	1	COUNT ENABLE
(OP2)	2	PRINT	04H	2	PRINT
	3	RESET E	08H	3	-
	4	INITIALIZE (LAMP)	10H	4	-
	5	-	20H	5	SOURCE COUNT OVERFLOW
	6	-	40H	6	-
	7	-	80H	7	-
INITIALIZE	(3,4)	RESET E + INIT (LAMP)	18H	(-)	No Read
8007 (OP3)	0	WRITE ONLY (FALSE/TRUE AL 1)			-
8007 (OP4)	0	WRITE ONLY (FALSE/TRUE AL 22)			-

a warm up, and this is the phase which is started by automatic restart.

Suitable counters determine the duration of each phase in multiples of 30 s. The measurement time (MT) is set by the operator in multiples of minutes. The number of measurements between calibrations (NM) is also prefixed by the operator.

The flow diagrams of Figs. 8, 9, and 10 will better explain the succession of phases.

Figure 8 illustrates the procedure "Poweron" which is self-explanatory up to the decisional block. The decision depends on the Automatic Power Restart Enabled or not. If not enabled the instrument goes to halt and waits for the operator. If APRE=1 the peripheral interface is activated and a "warm-up" flag is set in the operative field. Starting from that moment the operative field will govern all the operations, waiting for clocks that will set up following phases according to the flags that are set in succession by each one of the procedures. The phase duration is determined by suitable counters contained in the memory. The "Power-on" procedure allows one or two runs of Warm-up depending on the successfulness of the first calibration. For this purpose, counter W is set to 2. Counter WT is set initially to 20 to fix the warm-up time to 10 mins. The end of the procedure sets ENABLE flip-flop.

The interrupt procedure (Fig. 9) is calling one of the three procedures corresponding to the possible causes of interrupt, i.e., CLST, Pulses, Reco.

- Procedure CLST calls in turn procedure Clock or Stop. The Clock will be described later with the help of Fig. 10. Stop obviously will drive the system to the full stop if the operator requires that by pressing the pushbutton.
- Procedure Pulses executes simply the increment of suitable pulse counters that are contained in the RAM of the single-board computer.

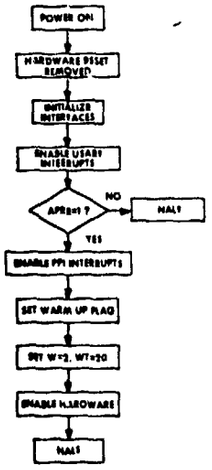

Fig. 8. Flow diagram corresponding to power-on. The program goes to halt and can only be started by keyboard if APRE=0. If APRE=1 the start is automatically done by clocks.

- Reco is a procedure that recognizes the first letter typed by the operator. He is allowed to type on the keyboard the following commands: Initialize, Start, Continue, Print, Test, Exper. Oper. He can actually type whatever he wants on the line; the program will recognize only the first letter and only if this letter is one of the initials listed above.

Power failure operation, not indicated in the diagram, is not software-implemented. When voltage decreases the circuit operates a permanent reset to the CPU and all the circuits.

Figure 10 reports the flow diagram corresponding to clock procedure. The peculiarity of this operation is that the operative field is written at the end of each phase so that one phase will prepare the call for the next one. The succession of the phases will be consequently obtained automatically as a daisy chain. As said, the first clock after power-on will find a warm-up flag in the operative field. The phases governed by the operative field are the following:

1. Warm up: WT is decreased up to zero and then W is decreased. At the same time MOV1 flag is set.

2. MOV1: This phase lasts 30 s and allows the sources to get their position near detectors. The first clock will then set "source count enable." This action is hardware prevented if the end of movement is not confirmed by optical position controllers (Fig. 11). If movement is okay, counter C1 is set to 2 that allows 1-minute source counting; if not, Alarm 23 is set.

3. Source counting: Two successive clocks will find this flag. When C1=0, source counters are disabled and counts are evaluated. At this point Alarm 22 flip-flop is written with "1" or "0" according to the evaluation. If counts are within limits Alarm 22 is set to zero and W is also reset. This means that if after the first warm-up time the calibration is okay, it is not necessary to allow for a second run of warm-up and calibration. If W was already zero, this reset is inefficient.

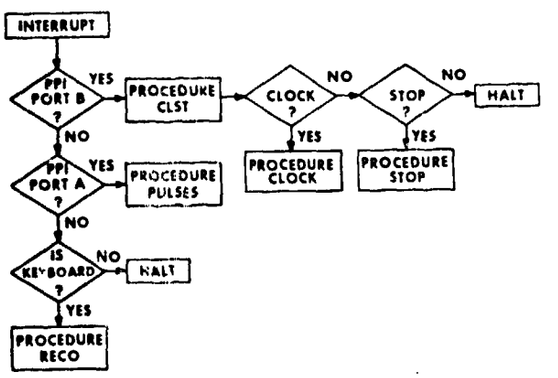

Fig. 9. Flow diagram corresponding to interrupt.

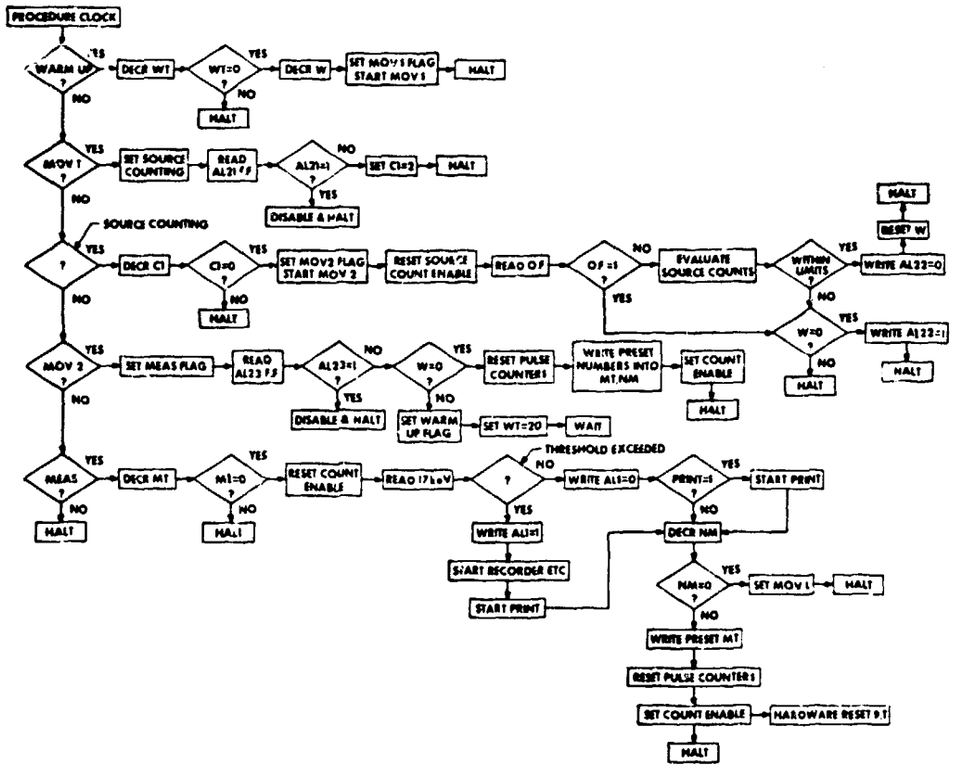

Fig. 10. Flow diagram of the clock action which is started by interrupt via procedure CLST. Clock procedure performs a third level polling before doing the proper action.

4. MOV2: Again, hardware will prevent the set-up of the measurement flag if MOV2 is not confirmed (Fig. 11). If the sources don't come back to their rest position, Alarm 23 is set. If movement is okay, first W is checked in order to know if a new warm-up is necessary. If not, pulse counters are reset and prefixed numbers are written into counters MT (measurement time) and NM (number of measurements between calibrations). Finally count enable is set.

5. Meas: Measurement flag means that pulses from the analog chains are counted. When MT reaches zero one measurement is performed and contents are evaluated. If threshold is exceeded, Alarm 1 is set and many actions are hardware initiated. Print of data is performed in this case. If threshold is not exceeded, print of data is performed only on request of the operator (procedure PRINT). The end of this subphase decreases counter NM and a new measurement is started. After the prefixed run of measurements, NM goes to zero and MOV1 is again set up.

The cycle continues endless.

8. Alarms

Different types of alarms will warn the operator if something will perform incorrectly during each phase. In these occurrences some actions will be automatically initiated. The various alarms with the consequent deeds are listed below:

ALARM 1 - This alarm is set up if the 17 keV counts in the selected time exceed the prefixed numerical threshold. Both time and threshold are stored in C-MOS memory. If Alarm 1 is found, the building computer is warned and some local actions are taken. A flashing yellow lamp is operated, and a double audible warning—local and remote—is started. (Audible devices can be silenced by the operator.) At the same time the data corresponding to 17 keV counts are sent to a chart recorder via a digital-to-analog converter (DAC), and the recorder is started. The recorder has a thermal pen writing because a normally idle instrument cannot safely use an inked pen. The contents of the three peak areas (17 keV, 59.6 keV, 400 keV) corrected with Eq. (2) are printed at the end of each alarmed measurement. The time of occurence of the alarm is not printed because it will result merely in a duplication of the real-time counting of the building computer and is also meaningless in case of power failure.

Last, but not least, Alarm 1 drives the holding tank controller. This is now only a provision that the hardware is already performing in view of the future construction of the holding tank and its controller. When this will be made, the effluent will be automatically diverted to the holding tank after the first occurrence of the alarm up to the end of the first non-alarmed measurement.

ALARM 2 - This alarm is set up during calibration and is in effect a group of three different alarms that take different actions.

— Alarm 21 is related to MOV1, and if the source position is not confirmed by an optical phaser, the action is to atop the instrument completely and warn the building computer. No recovery is possible without the intervention of the operator.

— Alarm 22 is related to source counting. If one or both source counters exceed their own high or low limits (stored in C-MOS memory) the action is simply a warning to the building computer. No printing or other automatic action is taken, but the operator can print out the source counting when needed. The instrument is not stopped, but there is no guarantee that the analog chain will perform correctly.

— Alarm 23 is related to MOV2 and is similar to Alarm 21.

ALARM 3 - This alarm is established by the lack of power and disables all the hardware in the instrument before the voltage is completely down, taking only the external action of warning the building computer.

9. Motor Drive Circuitry

The circuitry for driving the two sources near the detectors is shown in Fig. 11. A command given by the program sets the flip-flop MOV1 and starts the motion of the synchronous motor that drives the sources via a suitable demultiplication. When the sources reach the position, an optical coupler is operated and resets the flip-flop, stopping the motor. After calibration a similar action is performed by MOV2 flip-flop and the sources return to the rest position. The motor is always turning in the same sense, and the movement of the sources is circular. They are not entering and exiting the vessel but are contained in it. When they are in the far position, the mass of the support provides a sufficient screening. The two positions of the sources are identified by two diametrically opposed holes (lying on different radii) that allow the passing of the light beam when the right position is reached.

The time allowed for the movement is one clock, i.e., 30 s, while the movement is performed in 12 s.* This permits a full rotation of 360° in 24 s, that is less than a clock interval. This can be the case when power returns if a preceding power failure occurred when MOV2 was just initiated.

Each one of the flip-flops is driving a couple of AND gates connected in parallel to a command coming from the program. If the movement is properly terminated, the flip-flop has been reset, and the signal is routed to the proper action. If not, the command is routed to set the suitable alarm as explained in paragraph 8.

*Motor speed is 30 revolutions per second with a 60 Hz line, A 180:1 reduction gives an angular velocity of 10 rev/min. A suitable mechanical device transforms a complete revolution of the axis into a 90° displacement of the sources. The movement from rest to work position and vice versa is completed with a 180° rotation.

10. Interrupt and Dialog with the Operator

Three different lines can set up an interrupt to the system, but they share the only allowed interrupt level, i.e., RST7 of the SBC 80/10. Two lines come from one of the parallel interfaces and one from the serial link to the external terminal (USART).

The interrupt is first polled to recognize what port is calling. A multilevel polling is performed. When the port is recognized, a subsequent polling will realize what occurrence in that port is requesting service. A subsequent check will decide the action to be undertaken:

a) The first parallel input port is first polled to see if clock or stop is establishing the interrupt. In case of clock a third level of polling is performed, checking the content of the operative field before deciding the action to be taken.

b) The second parallel input port is simply polled to recognize which one of the SCAs is sending a pulse. The action is then to add one count to the corresponding counter.

c) The serial port is polled when a carriage return is sensed. In this case the first letter of the line will decide the procedure to be initiated. Messages such as "Illegal Command" or "Wrong Initial" are automatically printed if the operator is not requesting a foreseen action.

During the initialization a complete dialog between machine and operator is performed via an input/output terminal. When "Initialize" is recognized, the

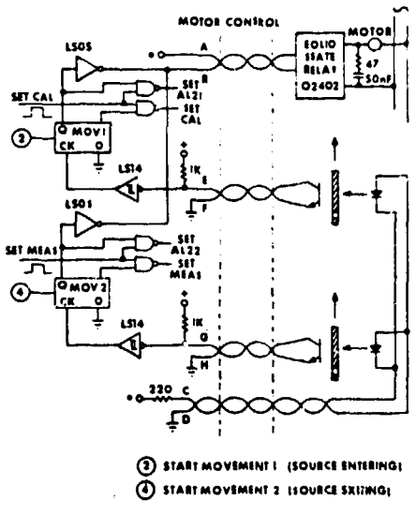

Fig. 11. Motor driving circuitry. The pulses indicated with #2 and 4 respectively are sent by the program via OP1 field. The light diodes will indicate the final position is reached and reset the corresponding flip-flop. The positive pulses will set the proper action or the alarm depending on the status of the flip-flop.

instrument prints automatically the value of the 11 operative constants that have been previously stored. Then 11 messages are printed in succession, each one waiting for an answer. The operator types simply an "X" if the particular stored constant is OK, or a number if a new value has to be stored into the C-MOS RAM. Special messages are printed if wrong action is taken by the operator. The numbers that the operator can change, if necessary, correspond to:

- Measurement time and number of successive measurements
- Threshold for the 17 keV integral counting
- Lower and upper limits for both source countings
- K constants for the three peak evaluation with Eq. (2)
- Number of successive measurements to be printed out (if any)

Two particular procedures can be established by the operator typing one of the following titles: Exper or Oper, or simply their initials. Exper is a procedure used during experimental phase that allows the operator to send recurrent pulses from the CPU to the hardware for test purposes and to read recurrent values from operative fields, C-MOS RAM and counters. Oper is described in the next chapter.

11. Software

The program has been written using the Intel PL/M high-level language. This language is stored in one of the computers of the computing center of the Laboratory and is accessible with input/output terminals. A powerful editor stored in the same machine allows for easy changes or additions to the program. The program is written as a series of declarations and a simple executable series of statements that invariably go to the same exit, where a halt is found waiting for interrupts.

Twenty-seven procedures have been written in PL/M language. They are then called as a daisy chain starting from the procedure called by the interrupt and control the operation as exposed in the preceding chapter. The easiness of writing the procedures that will then be called at the run time is a powerful means that is given by the PL/M language. A preceding work[6] made using the 8080 assembler resulted in a considerably longer development time, comparatively.

A peculiar characteristic of this program is the possibility given to the operator to write an auxiliary program in machine language and to store it into the RAM memory. A suitable procedure (OPER) of the main program will allow the acquisition of hexadecimal codes from the keyboard. When a "/" will be acquired, the auxiliary program will be automatically executed. This particular feature will allow future increase or modification without the need of rearranging completely the program using the PL/M compiler and chiefly will not require erasing and rewriting the PROMs. Some awkwardness due to ASCII code for the direct acquisition of hexadecimal digits will be described separately.[7]

I wish to make only a small consideration about the compiler, perhaps based on my hardware background. No particular care is taken by the compiler in case of HLT (halt). The only action is that the compiler automatically adds EI (enable interrupt) before HLT. With distinguished graciousness it adds another EI, HLT at the end of the program. So you are stopped, but you can easily restore the operation with the interrupt. True. My program is always at HLT waiting for interrupts but the interrupt will return, after servicing, to the next location. There are no exceptions: During execution all the instructions increment the program counter. So even with HLT the return is to the next instruction. The added statements EI, HLT work for the first time; thereafter, the program will pass as a hurricane into the RAMs. So it is necessary to create a jumping back loop after the HLT, for example like this:

```
.....
DECLARE EXIT LABEL;
.....
/* EXECUTABLE CODES*/
.....
GO TO EXIT;
.....
/* PROCEDURES*/
.....
/* INTERRUPT 7*/
.....
EXIT: HALT;
GO TO EXIT;
EOF
```

This seems to me quite obvious, but since I found many people surprised by this consideration, I wish in consequence to help those who will have doubts about it.

12. Conclusion

Figure 12 shows a picture of the digital part. The front panel has several lamps that help the operator in recognizing the various phases. Two lamps switched by the clock indicate enable state so the operator can have a clock indication. Also the measurement phase has two lamps that are switched at the beginning of each measurement, so the time of each run in this recurrent phase can be determined.

The total work has been made in several stages. First, the hardware, testing all circuits individually; second, the software, after a study of the compiler. The third step has been a simulation of the full operation with software means. The laboratory has the Intel INTERPB program stored in the computing center, and this is very useful for the possibility of simulating

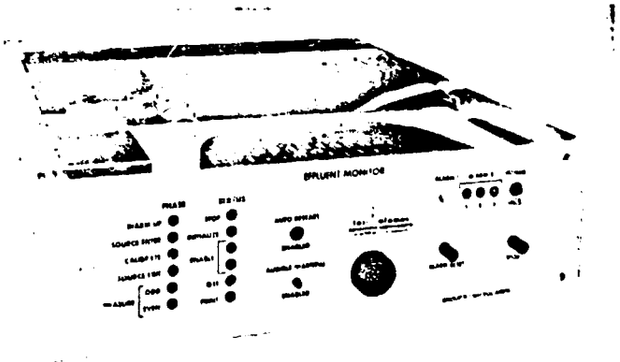

Fig. 12. Photograph of the digital controller. APR and audible warning enable switches are not accessible from front panel.

the various phases, including the interrupts. Finally, before loading the program into the PROMs, the program has been stored into RAMs, using the Intel SBC 80P loader.

The man-machine interaction is accomplished by a Teletype Mod. AS33 controlled by a suitable timer to allow power off when not operated and automatic start with any command. The teletypewriter will normally be idle so that a more sophisticated terminal would be redundant.

The full assembly with the analog part, the chart recorder, and the teletypewriter is shown in Fig. 13.

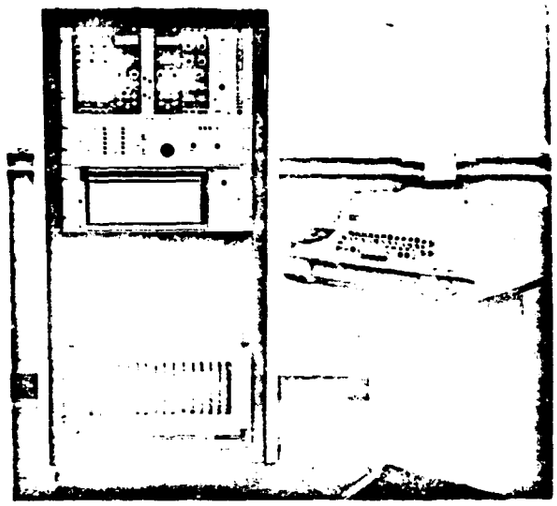

Fig. 13. View of the complete equipment.

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